DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	[illegible]	APPD
1	-	11-4-74	BP LRE	RWF MTS RFG
2A	-	1-5-76	MPPL LRE	CE LEG RFG
3A1	-	11-4-76	AS LRE	CE LEG RFG
4D1	-	8-31-77	NA TLB	CE LEG MG
5A		4-21-78	NA RLU	RAW JGC MG

SHEET INDEX

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CIRCUIT DESCRIPTION	5	3
	6	5

SYMBOL

TAPE UNIT CONTROLLER, 80 0
ELEMENT IDENT
A

TERM MOD	FUNCT	TERM	LOC
CARTWEO	I	201	2A3
CRCERO	I	114	2A2
DATDETO	I	219	3A7
DOINHO	I	014	3A7
FWDO	I	008	3A3
GPRO	I	108	2A3
INITBO	I	112	2A2
LPEWC	I	300	3A2
MAINT1	I	316	3A8
ROADJO	I	205	3A8
RWDINGAO	I	019	3A2
SSTO	I	117	2A0
STREQCO	I	105	2A0
TIMAO	I	118	3A6
T0RO	I	018	3A6
TTMSTPO	I	216	2A0
TTRDYO	I	301	2A4
TUCC0OEO	I	206	2A1
TUCRC1	I	015	2A1
WRITEC	I	110	2A6
CLK011	0	011	2H5
CLK021	0	016	2H6
ERO	0	006	2H2
GFO	0	303	2H4
INF080	0	214	3H4
INF090	0	315	3H6
INF100	0	317	3H6
INF110	0	017	3H8
INF120	0	217	3H8
INF130	0	218	3H1
INF140	0	013	3H3
INF150	0	012	3H0
LBEN1	0	101	2H2
MANENO	0	009	3H0
MODO	0	113	3H5
PSTAT1	0	106	2H1
ROYO	0	007	2H2
RWDINGBO	0	010	3H2
SYNCO	0	306	2H0
TIMBO	0	115	3H7
TTRDY1	0	302	2H4
WAITO	0	100	2H3
WRITEPO	0	109	2G9
B0TSTAT1	0I	107	3H3
E0TSTAT1	0I	111	3H3
INF060	0I	[illegible]	2H3
INF070	0I	[illegible]	2H4
LPEW1	0I	001	3H2
SSTAT1	0I	312	2H1
+5	P	000	3H4
+5	P	119	3H4
GRD	G	200	3H6
GRD	G	319	3H6

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

NOTES:

1. ⏚ GROUND RETURN

2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS

3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

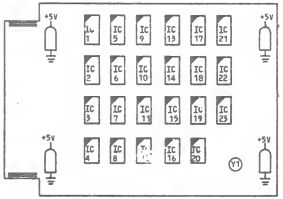
IC CODE	VCC TERM.	GRD TERM.
41AE	16	7,8
41BP	16	8
41BR	16	7,8
41CA	16	8
41CC	16	7,8
41CJ	16	8
41DL	16	8
41U	16	8
41W	16	8
41B0	9	16

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	119,000
GRD	319,200

5. HORIZONTAL MOUNTING CENTERS AT 1.00 INCH.

6. INTEGRATED CIRCUIT LOCATION GUIDE: (COMPONENT SIDE SHOWN).



UNNUBMERED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK19
CONNECTOR ON FRAME	947A OR 947C
ACCEPTABLE SERIES	6

CURRENT DRAIN: 405ma

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE
5A

1N98

JK19 CIRCUIT PACK

CARTRIDGE TAPE TRANSPORT CONTROLLER, BOARD 0
CIRCUIT

②

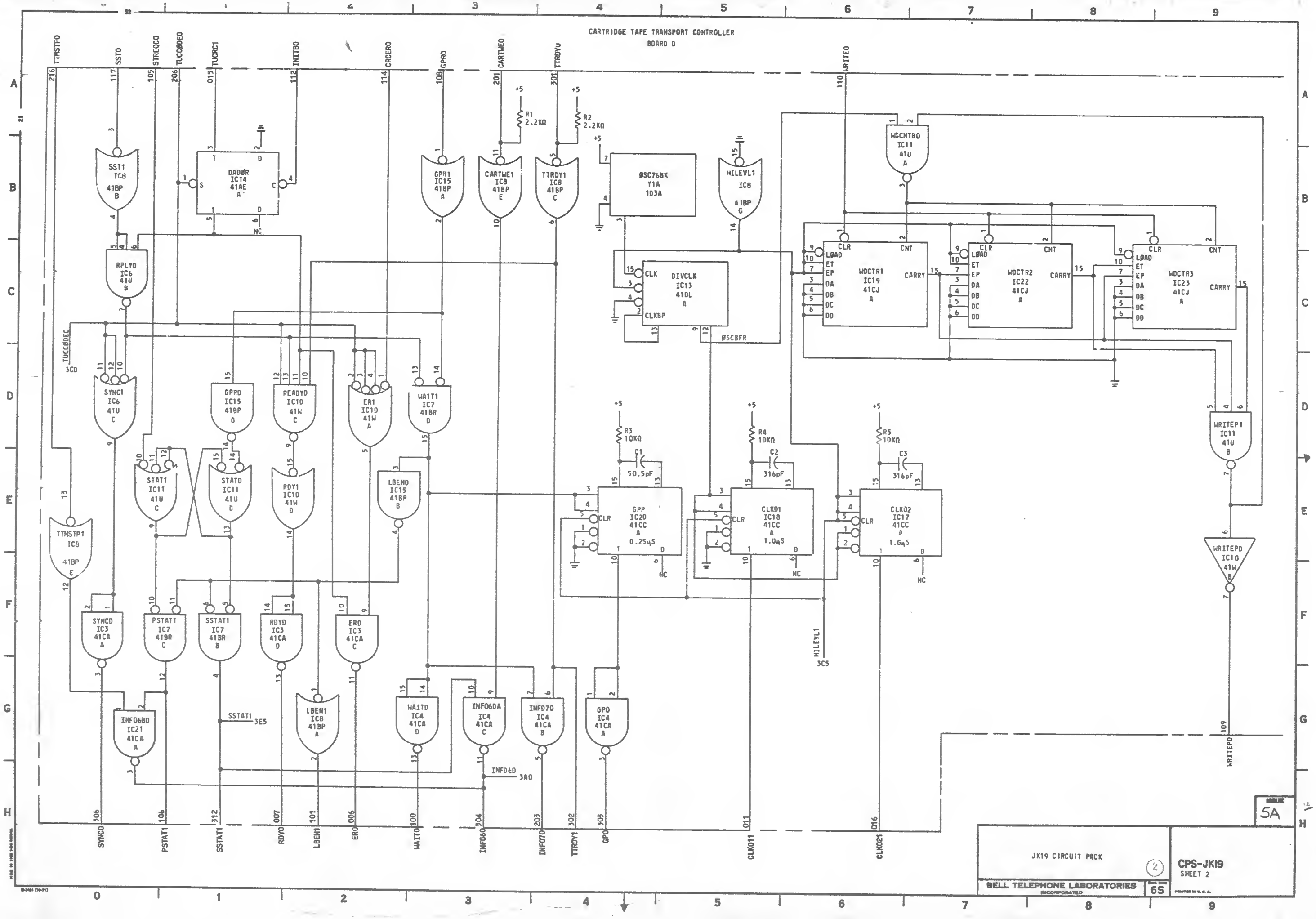
AT&TCO
STANDARD

CPS-JK19
6 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

CARTRIDGE TAPE TRANSPORT CONTROLLER
BOARD D



ISSUE 5A

JK19 CIRCUIT PACK

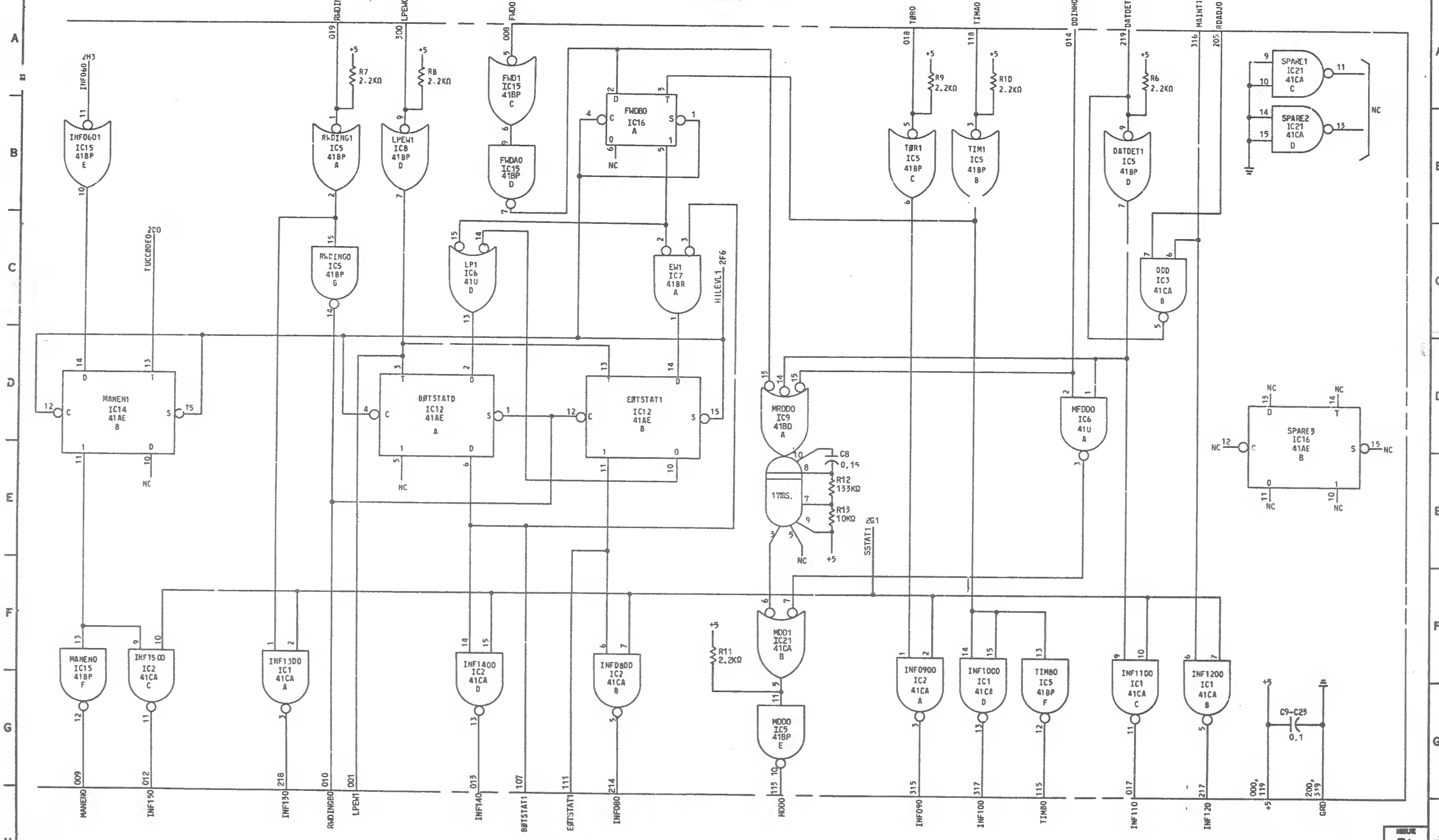
②

CPS-JK19
SHEET 2

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

CARTRIDGE TAPE TRANSPORT CONTROLLER
BOARD 0



ISSUE
5A

JK19 CIRCUIT PACK

CPS-JK19
SHEET 3

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE	IC1 41CA		IC2 41CA		IC3 41CA		IC4 41CA		IC5 41BP		IC6 41U	
ELEM ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	INF1300	3G1	INF0900	3G6	SYNC0	2F0	GP0	2G4	RWOING1	3B2	MFDD0	307
B	INF1200	3G8	INF0800	3G4	ODD	3C8	INF070	2G4	TIM1	3B6	RPLY0	2C0
C	INF1100	3G8	INF1500	3G0	ER0	2F2	INF060A	2G3	TØR1	3B6	SYNC1	200
D	INF1000	3G6	INF1400	3G3	ROY0	2F2	WAIT0	2G3	OATDLT1	3B7	LP1	3C3
E									MDD0	3G5		
F									TIMB0	3G7		
G									RWDING0	3C2		

LOC CODE	IC7 41BR		IC8 41BP		IC9 41BD		IC10 41W		IC11 41U		IC12 41AE	
ELEM ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	EW1	3C4	LBEN1	2C2			ER1	2D2	WOCNTBD	2A6	BØTSTAT0	307
B	SSTAT1	2F1	SST1	2B0	MRDD0	3E5	WRITEP0	2E9	WRITEP1	209	EØTSTAT1	304
C	PSTAT1	2F1	TTRDY1	2B4			READY0	202	STAT1	2ED		
D	WAIT1	203	LPEW1	3B2			RDY1	2E2	STATD	2E1		
E			CARTWE1	2B3								
F			TTMSTP1	2E0								
G			HILEVL1	2B5								

LOC CODE	IC13 410L		IC14 41AE		IC15 41BP		IC16 41AE		IC17 41CC		IC18 41CC	
ELEM ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	DIVCLK	2C5	OADØR	2B1	GPR1	2B3	FWDB0	3A4	CLK02	2E6	CLKD1	2E5
B			MANEN1	3DD	LBEN0	2E2	SPARE 3					
C					FWD1	3A3						
D					FWDA0	3B3						
E					INF06C1	3B0						
F					MANEN0	3G0						
G					GPP0	2D1						

LOC CODE	IC19 41CJ		IC20 41CC		IC21 41		IC22 41CJ		IC23 41CJ	
ELEM ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	WDCTR1	2C6	GPP	2E4	INF06B0	2G0	WOCTR2	2C7	WDCTR3	2C9
B					MDD1	3F5				
C					SPARE1					
D					SPARE2					
E										
F										
G										

CAPACITOR

DESIG	CODE
C1	KS-20813 L2,50.5PF
C2,C3	KS-20813 L4,316PF
[4]C4-C7	601A,5
C8	KS-20300 L1,0.15
[15]C9-C23	KS-21901 L1,0.1

CLOCK OSCILLATOR

DESIG	CODE
Y1A	103A 768.000KHZ

RESISTOR

DESIG	CODE
R1,R2	KS-20616 L1A,2200
[4] R3-R5,R13	KS-20616 L1A,10KΩ
[6] R6-R11	KS-20616 L1A,2.2KΩ
R12	KS-20616 L1A,162KΩ

ISSUE
5A

JK19 CIRCUIT PACK
②

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

CPS-JK19
SHEET 4

PRINTED IN U.S.A.

CIRCUIT DESCRIPTION

A. FUNCTIONAL DESCRIPTION

JK19 IS ONE OF THE FOUR BOARDS WHICH MAKE UP THE CARTRIDGE TAPE TRANSPORT CONTROLLER (CTTC). THIS BOARD CONTAINS MOST OF THE HANDSHAKING LOGIC, THE 2-PHASE WRITE CLOCK, WRITE DELAY TIMING, AND MOST OF THE SECONDARY STATUS OUTPUTS. A BLOCK DIAGRAM OF JK19 IS SHOWN IN FIG. 1.

THE CTTC ADDRESS LATCH ENABLES THE SPI AND BT HANDSHAKING LOGIC WHENEVER THE SERIAL PERIPHERAL INTERFACE (SPI) TRANSMITS A COMMAND TO THE CTTC. IT MAINTAINS THE ENABLE STATE UNTIL A COMMAND IS ISSUED FROM THE SPI WHICH DOES NOT CARRY THE CTTCs DEVICE CODE, OR A TDC INITIALIZE COMMAND IS ISSUED.

THE SPI AND BT HANDSHAKING LOGIC WHICH IS ENABLED BY THE CTTC ADDRESS LATCH, GENERATES THE PROPER HANDSHAKING SIGNALS WHEN THE CTTC RECEIVES A COMMAND OR A STATUS REQUEST FROM THE SPI. THE SYNCO AND ERO ARE ENABLED, INDICATING TO THE SPI THAT THE COMMAND WAS RECEIVED WHENEVER THE CTTC COMMAND LEAD IS ENABLED. SYNCO WILL RETURN TO ITS DISABLED STATE AT THE TRAILING EDGE OF THE COMMAND PULSE. IF THE CRC CIRCUIT LOCATED ON JK17 IS IN AN ERROR CONDITION, THE ERO LEAD WILL REMAIN ENABLED UNTIL THE CTTC IS TAKEN OFF-LINE (THE ADDRESS LATCH IS DISABLED) OTHERWISE, IT RETURNS TO ITS DISABLED STATE AT THE TRAILING EDGE OF THE COMMAND PULSE. WHEN THE CTTC IS ADDRESS (ON-LINE) AN ACTIVE SIGNAL ON THE STATUS-REQUEST LEAD WILL CAUSE A PULSE ON THE GENERATE-PARITY LEAD, AND ENABLES THE WAITO AND SYNCO LEADS. THE PULSE ON THE GENERATE-PARITY LEAD IS FED TO THE BUS TERMINATOR (BT) CIRCUIT, REQUESTING THAT PARITY BE GENERATED FOR THE 16 BITS OF STATUS INFORMATION THE CTTC HAS LOADED ONTO THE BUS ENABLING WAITO INDICATES TO THE SPI THAT THE STATUS INFORMATION IS NOT READY. WHEN THE BT CIRCUIT HAS RECEIVED THE STATUS INFORMATION FROM THE BUS, IT WILL GENERATE A PULSE WHICH WILL APPEAR ON THE GENERATE-PARITY REPLY LEAD. THIS PULSE CAUSES THE SPI AND BT HANDSHAKING LOGIC TO DISABLE THE WAITO LEAD AND REMOVE THE STATUS INFORMATION (INFORMATION WHICH WAS LOADED INTO THE BUS BY THE CTTC WHEN THE STATUS REQUEST COMMAND WAS RECEIVED) FROM THE BUS. AT THIS POINT THE BUSs WAITO LEAD HAS BEEN ENABLED BY THE BT CIRCUIT. AS SOON AS PARITY IS CALCULATED BY THE BT CIRCUIT, THE CTTs STATUS, ALONG WITH PROPER PARITY, WILL BE GATED ONTO THE BUS BY THE BT CIRCUIT. THE WAITO LEAD WILL BE DISABLED, INDICATING TO THE SPI THAT THE INFORMATION IS READY. AS THIS INFORMATION IS RETRIEVED BY THE SPI, THE ACTIVE SIGNAL ON THE STATUS-REQUEST LEAD IS REMOVED CAUSING THE SYNCO LEAD TO BE DISABLED.

THE MANUAL-ENABLE LATCH IS ENABLED WHENEVER THE CTTC RECEIVES A COMMAND WHILE THE MANUAL-ENABLE LEAD (INF060) IS ENABLED. THE OUTPUT OF THE MANUAL-ENABLE LATCH IS FED DIRECTLY TO THE CTT AND ENABLES THE MANUAL PUSHBUTTONS WHEN ACTIVE.

THE STATUS GATING CIRCUIT LOADS CTT STATUS INFORMATION ONTO THE BUS (TO BE ACCEPTED BY THE BT CIRCUIT). WHEN IT IS ENABLED BY A STATUS REQUEST COMMAND, IT ALSO FEEDS OTHER CTTC CIRCUITS WITH OPERATING STATUS INFORMATION, TAPE IN MOTION, DATA DETECT AND REWINDING STATUS.

THE TAPE POSITION STATUS CIRCUIT MAINTAINS A STATUS OF THE POSITION OF THE MAGNETIC TAPE, WITHIN THE TAPE CARTRIDGE. ITS OUTPUTS (INF080 AND INF140) INDICATE WHETHER THE HEAD IS BETWEEN THE LOAD POINT AND EARLY WARNING MARKERS OR AT EITHER END. DATA SHOULD ONLY BE WRITTEN ONTO TAPE BETWEEN THESE TWO MARKERS.

THE 2-PHASE OSCILLATOR PROVIDES A 2-PHASE CLOCK FOR WRITING DATA ONTO TAPE. THE 2-PHASE CLOCK OUTPUT OPERATES AT 48KHZ GENERATING 1μs CLOCK PULSES FIG. 2. THE OSCILLATOR CLOCK ALSO FEEDS A 96KHZ SQUARE WAVE INTO THE WRITE DELAY CIRCUIT. THE WRITE DELAY CIRCUIT WHEN TRIGGERED BY A WRITE COMMAND, WILL GENERATE A 42.59ms PULSE AT ITS OUTPUT WHICH IS USED TO INITIALIZE THE WRITE CIRCUITS LOCATED ON JK1B.

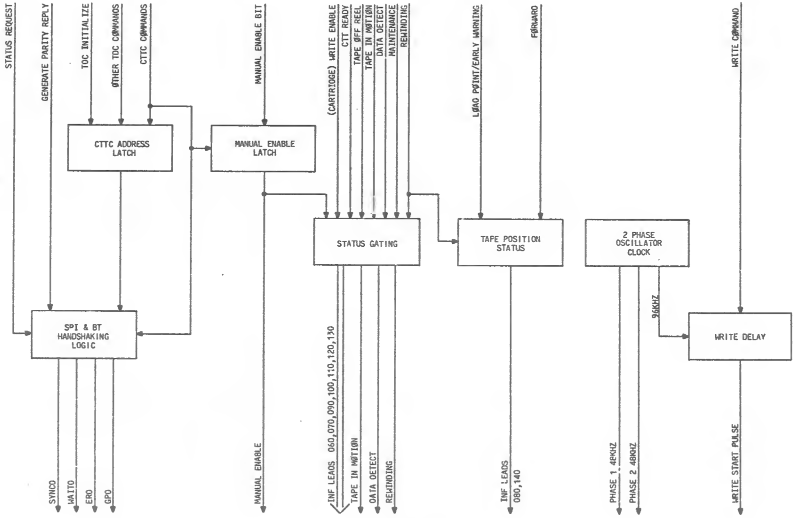


FIGURE 1 - BLOCK DIAGRAM

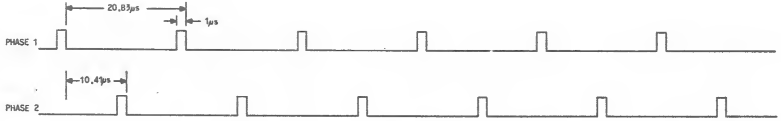


FIGURE 2 - 2PHASE CLOCK

ISSUE
3AI

JK19 CIRCUIT PACK ②

CPS-JK19
SHEET 5

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PRINTED IN U.S.A.

CIRCUIT DESCRIPTION (CONT)

B. DETAILED DESCRIPTION

IN RESPONSE TO EVERY COMMAND ISSUED BY THE SPI, CIRCUITS LOCATED ON JK16 WILL GENERATE A HIGH-GOING PULSE THAT APPEARS ON THE [illegible]RC1 LEAD. THE PULSES APPEARING ON THIS LEAD WILL ATTEMPT TO TOGGLE THE D-TYPE FLIP-FLOP, DADØR, TO ITS CLEARED STATE. CIRCUITS LOCATED ON JK16 GENERATE A LOW-GOING PULSE ON THE TUCCØDED LEAD WHEN THE COMMAND, ISSUED BY THE SPI, IS DIRECTED TO THE CTTC. THIS PULSE WILL ALWAYS LEAVE DADØR IN ITS SET STATE. COMMANDS ISSUED TO THE CTTC WILL LEAVE DADØR IN ITS SET (ON-LINE) STATE AND COMMANDS NOT DIRECTED TO THE CTTC, WILL LEAVE DADØR IN ITS CLEARED (OFF-LINE) STATE. WHEN A TDC INITIALIZE COMMAND IS ISSUED BY THE SPI, THE CIRCUITS LOCATED ON JK16 WILL GENERATE A LOW-GOING PULSE ON THE INITBO LEAD. THIS PULSE WILL ALWAYS LEAVE DADØR IN ITS CLEARED (OFF-LINE) STATE. PULSES ON THE TUCCØDEO LEAD WILL APPEAR ON THE SYNCO LEAD AFTER PROPAGATING THROUGH SYNC1 AND SYNCO. THE LOW-GOING PULSE ON THE SYNCO LEAD IS FED BACK TO THE SPI, INDICATING THAT THE COMMAND WAS RECEIVED BY THE CTTC. THE PULSE ON THE TUCCØDEO LEAD ALSO APPEARS ON THE ERO LEAD AFTER PROPAGATING THROUGH ER1 AND ERO. NOTICE THAT THE ONE OUTPUT OF DADØR GOES HIGH AT THE LEADING EDGE OF THE TUCCØDEO PULSE, ENABLING ERO. FINALLY, THE TUCCØDEO SIGNAL WHILE AT A LOW LEVEL DISABLES READYO. WHEN THE CCT IS IN A READY STATE, ITS READY-STATUS LEAD TTRDYD WILL BE AT A LOW LEVEL. THIS MAINTAINS A HIGH LEVEL AT THE TTRDY1 INPUT TO READYO. IF THE CTT IS IN A READY STATE, THE DISABLING OF READYD WILL CREATE A LOW-GOING PULSE WHICH PROPAGATES THROUGH RDY1 AND RDYO. THE SSTD LEAD IS DRIVEN LOW BY THE SPI TO GET EACH COMMAND REPLY. A LOW LEVEL INPUT FORCES THE OUTPUT OF SST1 HIGH. IF THE CTTC IS ON-LINE, THE ONE OUTPUT OF DADØR WILL BE AT A HIGH LEVEL WHICH ENABLES RPLYO. THE ENABLED OUTPUT OF RPLYO, WILL BE DRIVEN LOW, BY THE HIGH-OUTPUT OF SST1. THIS LOW-OUTPUT DRIVES THE OUTPUT OF SYNC1 HIGH FORCING THE OUTPUT OF SYNCD LOW. THE LOW OUTPUT OF RPLYO DISABLES READYO, CREATING A HIGH LEVEL AT THE OUTPUT OF RDYD. SINCE THE INPUT GPRO IS NORMALLY AT A HIGH LEVEL, IT MAINTAINS A LOW LEVEL AT THE OUTPUT OF GPR1, ENABLING WAIT1. THE LOW LEVEL FROM RPLYD WILL DRIVE THE OUTPUT OF WAIT1 HIGH. THIS HIGH LEVEL FORCES THE OUTPUT OF WAITO AND LBEND LOW AND ENABLES INF070. THE LOW LEVEL ON WAITO IS AN INDICATION TO THE SPI THAT STATUS INFORMATION IS NOT READY. ENABLING OF INF070 GATES THE READY STATUS OF THE CTT ONTO THE BUS. WHEN THE CTT IS IN A READY STATE, IT MAINTAINS A LOW LEVEL ON THE TTRDYO LEAD WHICH DRIVES THE OUTPUT OF TTRDY1 HIGH. THIS OUTPUT FEEDS INF070. THE LOW OUTPUT OF LBEND FORCES THE OUTPUT OF PSTAT1 OR SSTAT1 HIGH, DEPENDING UPON WHICH ONE IS ENABLED BY THE SR FLIP-FLOP, STAT1/STATD. IN ITS NORMAL STATE, THIS FLIP-FLOP WILL MAINTAIN A LOW LEVEL AT THE OUTPUT OF STAT1 ENABLING PSTAT1 PROVIDED THE NORMAL OR PRIMARY STATUS REPLY IS REQUESTED. TO RETRIEVE THE SECONDARY STATUS, A PULSE GENERATED BY CIRCUITS LOCATED ON JK16 WOULD HAVE APPEARED ON THE STREQCD LEAD, WHEN THE LAST COMMAND WAS ISSUED TO THE CTTC (STATUS REQUEST COMMAND). THIS PULSE SETS THE FLIP-FLOP STAT1/STATO, SO THAT THE OUTPUT OF STATO IS LOW ENABLING SSTAT1. A HIGH OUTPUT FROM PSTAT1 ENABLES INF06B0 AND IS FED TO OTHER CIRCUITS IN THE CTTC. A HIGH OUTPUT FROM SSTAT1 (SECONDARY STATUS) ENABLES INF060A, INF0800, INF0900, INF1000, INF1100, INF1200, INF1[illegible], INF1400, AND INF1500. ALL THE ABOVE GATES ARE USED TO LOAD STATUS INFORMATION ONTO THE BUS WHEN THEY ARE ENABLED BY SSTST1.

IN ADDITION, AS THE OUTPUT OF WAIT1 GOES HIGH, IT TRIGGERS THE MONOPULSER GPP. THIS GENERATES A 0.25μs HIGH-GOING PULSE TO APPEAR AT THE OUTPUT OF GPD. THE OUTPUT OF GPO IS FED TO THE BUS TERMINATOR (BT) CIRCUIT ON JK8 AND JK9. IT IS A SIGNAL TO THE BT CIRCUIT THAT STATUS INFORMATION HAS BEEN LOADED ONTO THE BUS AND THAT PARITY SHOULD BE GENERATED FOR THE SAME. (A HIGH LEVEL ON EITHER SSTAT1 OR PSTAT1 ENABLES THE GATES WHICH LOAD THE STATUS INFORMATION ONTO THE BUS.) AFTER THE INFORMATION HAS BEEN RECEIVED BY THE BT CIRCUIT, THE GPRO LEAD WILL BE DRIVEN LOW BY THE BT CIRCUIT. THIS LOW LEVEL CAUSES THE OUTPUT OF GPR1 TO GO HIGH. THE HIGH OUTPUT OF GPR1 DISABLES WAIT1 THEREBY, DISABLING INF070 AND ALLOWING THE OUTPUT OF WAITO TO GO HIGH. IN REALITY, THE OUTPUT OF WAITD REMAINS LOW BECAUSE WAITO IS AN OPEN COLLECTOR TYPE GATE AND THE BT CIRCUIT WHICH IS NOW CONTROLLING THE BUS, HOLDS ITS OUTPUT LEAD LOW. THE LOW OUTPUT OF WAIT1 ALSO DRIVES THE OUTPUT OF LBENO HIGH DISABLING PSTAT1 AND SSTAT1. WITH THESE TWO GATES DISABLED, ALL STATUS LOADING OF THE BUS BY THE CTTC IS INHIBITED. THE HIGH-LEVEL AT THE OUTPUT OF GPR1 ALSO DRIVES THE OUTPUT OF GPRO LOW SETTING THE OUTPUT OF STATO TO A HIGH LEVEL AND STAT1 TO A LOW LEVEL (NORMAL STATE OF STAT1/STATD). AFTER THE BT CIRCUIT HAS CALCULATED THE CORRECT PARITY AND TRANSMITTED THE STATUS INFORMATION TO THE SPI, IT WILL DRIVE THE GPRO INPUT LEAD HIGH AND THE SPI WILL DRIVE SSTO HIGH. THE HIGH INPUT ON SSTO ALLOWS SYNCO TO GO HIGH AND READYO IS AGAIN ENABLED SO THAT RDYO WILL GO LOW, ASSUMING THAT TTRDYO IS AT A LOW LEVEL.

FOR PRIMARY STATUS PSTAT1 IS HIGH ENABLING INF06B0. TTMSTPO IS DRIVEN TO A LOW LEVEL BY THE CTT WHEN THE CTT IS IN A MAINTENANCE-STOP STATE. THIS LOW OUTPUT DRIVES THE OUTPUT OF TTMSTP1 HIGH. THE OUTPUT OF TTMSTP1 FEEDS INF06B0 TO LOAD THE INF06D BUS LEAD. NOTICE INF06B0 AND INF06DA ARE OPEN COLLECTOR GATES. FOR SECONDARY STATUS SSTAT1 IS HIGH ENABLING ALL SECONDARY STATUS GATING. CARTWEO IS DRIVEN LOW BY THE CTT WHEN THE CTTs CARTRIDGE IS WRITE ENABLED. THE OUTPUT OF CARTWE1 WHICH IS DRIVEN HIGH BY THIS LOW INPUT, FEEDS INF[illegible]0A. INF0800 AND INF1400 ARE FED BY THE TWO D-TYPE FLIP-FLOPS EØTSTAT1 AND BØTSTATD, RESPECTIVELY. THE FUNCTIONS OF THESE TWO FLIP-FLOPS WILL BE DESCRIBED BELOW.

THE INPUT TØRO IS DRIVEN LOW BY THE CTT WHEN THE CTTs CARTRIDGE TAPE IS OFF EITHER REEL. THE OUTPUT OF TØR1 WHICH IS DRIVEN HIGH BY THIS INPUT, FEEDS INF090. THE INPUT TIMAO IS DRIVEN LOW BY THE CTT WHEN THE CTT IS IN MOTION. THE OUTPUT OF TIM1, WHICH IS DRIVEN HIGH BY THIS LOW INPUT, FEEDS INF1000. THE INPUT, DATDETO, IS DRIVEN LOW BY THE CTT WHEN THE CTTs READ WINDING IS MOVING OVER DATA ON THE TAPE. THE OUTPUT OF DATDET1, WHICH IS DRIVEN HIGH BY THIS LOW INPUT, FEEDS INF1100. THE OUTPUT OF DATDET1 ALSO DRIVES TWO OTHER GATES MFDDO (MODIFIED FORWARD DATA DETECT) AND MRDDO (MODIFIED REVERSE DATA DETECT) WHICH ARE COMBINED TO CREATE MDDO. DDINHD IS PULSED LOW FOR 30ms BY CIRCUITS LOCATED ON JK16 AS ANY READ-A-BLOCK, WRITE, OR BACKSPACE OPERATION IS INTIATED. THE OUTPUT OF MDDO IS FED TO OTHER CTTC CIRCUITS TO BE USED FOR READ, WRITE, AND MOTION CONTROL. MRDDO IS A 17ms TIME DELAY CIRCUIT ENABLED BY THE TAPE MOVING IN THE REVERSE DIRECTION (FWDAO). IT IS USED TO DELAY CLEARING THE MOTION REGISTER ON JK16 WHEN THE TAPE ENTERS AN INTER RECORD GAP GOING BACKWARDS. THIS GUARANTEES THAT THE TAPE WILL BE UP TO SPEED ON A REREAD ATTEMPT WITH WORST CASE MINI-RECORDER RAMPS AND SPEED.

DATDETO CAN ALSO BE DRIVEN LOW BY DDO. BOTH DDO AND THE CTTs GATE, WHICH DRIVES DATDETO, ARE OPEN COLLECTOR GATES. THE OUTPUT OF DDO IS DRIVEN LOW BY HIGH LEVELS ON BOTH MAINT1 AND RDADJO. MAINT1 WHICH ALSO FEEDS INF1200 IS HELD AT A HIGH LEVEL BY CIRCUITS LOCATED ON JK16, WHEN THE CTTC IS IN ITS MAINTENANCE STATE. RDADJO IS DRIVEN HIGH BY THE WRITE CIRCUIT LOCATED ON JK1B AT THE BEGINNING OF ANY WRITE OPERATION. IT IS FORCED BACK TO A LOW LEVEL AT THE END OF EACH WRITE OPERATION. THE ABOVE EXPLANATION MEANS THAT WHEN A MAINTENANCE WRITE OPERATION IS PERFORMED, THE WRITE CIRCUITS WILL IMPOSE A FALSE DATA DETECT SIGNAL TO THE INPUT OF DATDET1. THE INPUT RWDINGAO IS DRIVEN LOW BY THE CTT WHEN THE CTT IS IN A REWIND SEQUENCE. THE OUTPUT OF RWDING1 WHICH IS DRIVEN HIGH BY A LOW LEVEL ON RWDINGAO, FEEDS INF1300. THIS HIGH OUTPUT FROM RWDING1 ALSO FORCES THE OUTPUT OF RWDINGO LOW THE OUTPUT OF RWDINGO IS FED INTO THE TAPE POSITION STATUS CIRCUIT AND IT IS USED BY OTHER CTTC CIRCUITS FOR FUNCTIONAL CONTROL.

THE MANUAL ENABLE LATCH IS THE D-TYPE FLIP-FLOP, MANEN1. IT IS TOGGLED TO A SET STATE WHENEVER THE CTTC RECEIVES AN ORDER (PULSE ON THE TUCCØDEO LEAD), WHILE INF060 IS AT A LOW LEVEL (ONE STATE). THE LOW LEVEL ON INF06D MAINTAINS A HIGH LEVEL AT THE OUTPUT OF INF06D1 WHICH FEEDS THE DATA INPUT TO MANEN1. MANEN1 IS CLEARED BY A CTTC COMMAND WHEN INF06D IS IN ITS ZERO STATE. THE HIGH LEVEL AT THE ONE OUTPUT OF MANEN1 FORCES THE OUTPUTS OF MANEND AND INF1500 (WHEN IT IS ENABLED BY SSTAT1) LOW. THE OUTPUT OF MANENO IS FED DIRECTLY TO THE CTT. WHEN IT IS AT A LOW LEVEL, THE MANUAL PUSH-BUTTONS ON THE CTT ARE ENABLED.

THE TAPE POSITION STATUS CIRCUIT, WHICH MAINTAINS A STATUS OF THE POSITION OF THE MAGNETIC TAPE WITHIN THE TAPE CARTRIDGE, INCLUDES THREE D-TYPE FLIP-FLOPS BØTATATO, EØTSTAT1, AND FWDBO FOR ITS MEMORY. WHEN THE CTT IS BEING INITIALIZED BY A REWIND SEQUENCE, RWDINGAO WILL BE HELD LOW BY THE CTT UNTIL THE SEQUENCE IS COMPLETED. THE LOW LEVEL AT THE RWDINGAO INPUT CREATES A LOW LEVEL AT THE SET INPUT OF BØTSTATD AND AT THE CLEAR INPUT OF EØTSTAT1. THE FWDBO FLIP-FLOP STORES THE STATE OF THE FWDO LINE (FROM THE MOTION REGISTER ON JK16) EACH TIME TAPE IN MOTION (TIM1) GOES ACTIVE. WHEN THE REWIND SEQUENCE IS COMPLETED RWDINGAO RETURNS TO A HIGH LEVEL, BØTSTATO WILL BE IN ITS SET STATE AND EØTSTAT1 WILL BE IN ITS CLEARED STATE. THIS STATE OF THE TWO FLIP-FLOPS INDICATES THAT THE TAPE IS POSITIONED SO THAT THE CTT HEAD IS IN THE WRITEABLE AREA, BETWEEN THE LOAD POINT (LP) AND THE EARLY WARNING (EW) MARKERS ON THE TAPE. (A REWIND SEQUENCE STOPS THE TAPE JUST PAST THE LOAD POINT MARKERS.) THE READER SHOULD NOTE THAT LPEWO IS PULSED LOW BY THE CTT EACH TIME EITHER THE LP OR THE EW MARKER CROSSES THE CTT SENSOR. THE PULSE ON THE LPEWO LEAD WILL CREATE A PULSE AT THE OUTPUT OF LPEW1 WHICH IS FED INTO THE TOGGLE INPUT OF BOTH BØTSTATO AND EØTSTAT1. THIS TOGGLE PULSE WILL CAUSE BØTSTATO TO GO TO ITS CLEARED STATE. EØTSTAT1 WILL NOT CHANGE STATES. NOTICE THAT AT THE TIME THE TOGGLE PULSE OCCURRED, THE HIGH LEVEL AT THE OUTPUT OF THE FWDO F-F AND THE HIGH LEVEL AT THE OUTPUT OF EØTSTAT1, MAINTAINED A LOW LEVEL AT THE OUTPUT OF LP1. THE OUTPUT OF LP1 FEEDS THE DATA INPUT TO BØTSTATO. THE DATA INPUT TO EØTSTAT1 IS FED BY EW1 WHOSE OUTPUT WAS HELD LOW BY THE HIGH LEVEL ON FWDBO. THE CLEARED STATE OF BOTH BØTSTATO AND EØTSTAT1 INDICATE THAT THE TAPE IS POSITIONED SO THAT THE CCT HEAD IS OUT OF THE WRITEABLE AREA OF THE TAPE, NEAR THE BEGINNING OF TAPE. AFTER BEING STOPPED, IF THE TAPE IS MOVED IN THE FORWARD DIRECTION, THE OUTPUT OF THE FWDBO F-F WILL BE DRIVEN LOW BY THE COMBINATION OF FWDO COMMAND AND TIM1. THIS WILL MAINTAIN A HIGH LEVEL AT THE DATA INPUT OF BØTSTATO. THE HIGH LEVEL AT THE OUTPUT OF BØTSTATD MAINTAINS A LOW LEVEL AT THE DATA INPUT OF EØTSTAT1. AS THE LP MARKER CROSSED THE CTTs SENSOR, A PULSE WILL APPEAR ON THE LPEWO LEAD. THIS PULSE WILL TOGGLE BØTSTATO TO ITS SET STATE AND HAVE NO EFFECT ON EØTSTAT1. AGAIN THE TAPE IS POSITIONED SO THAT THE CTTs HEAD IS OVER THE WRITEABLE AREA OF TAPE. BØTSTATO IS SET AND EØTSTAT1 IS CLEARED. IF THE TAPE IS MOVED IN THE FORWARD DIRECTION SO THAT THE EW MARKER PASSES THE CTTs SENSOR, A PULSE WILL AGAIN APPEAR ON THE LPEWO LEAD. SINCE BØTSTATO IS SET AND FWDBO IS LOW AS THIS PULSE OCCURES, THE DATA INPUT TO BOTH BØTSTATO AND EØTSTAT1 WILL BE AT A HIGH LEVEL, ALLOWING BØTSTATD TO REMAIN SET AND EØTSTATO TO BE TOGGLED TO ITS SET STATE. THE SET STATE OF BOTH THESE FLIP-FLOPS INDICATE THAT THE CTTs HEAD IS OUTSIDE THE WRITEABLE AREA OF TAPE NEAR THE END OF TAPE. IF THE TAPE IS STOPPED AND PUT IN REVERSE, THE FWDO LEAD WILL BE HELD AT A HIGH LEVEL BY JK16. THIS HIGH LEVEL IN COMBINATION WITH TIM1 GOING ACTIVE AGAIN WILL CLEAR THE FWDBO F-F AND MAINTAIN A LOW LEVEL AT THE DATA INPUT TO EØTSTAT1. THE "0" OUTPUT OF EØTSTAT1 MAINTAINS A HIGH LEVEL AT THE OUTPUT OF LP1 WHICH IS FED INTO THE DATA INPUT OF BØTSTATD. WHEN THE EW MARKER PASSES THE CTTs SENSOR, A PULSE WILL OCCUR ON THE LPEWO LEAD. THIS PULSE WILL LEAVE BØTSTAT IN ITS SET STATE AND TOGGLE EØTSTAT1 TO ITS CLEARED STATED. AGAIN, THE CTTs HEAD IS OVER THE WRITEABLE AREA OF TAPE (BØTSTATO IS SET AND EØTSTAT1 IS CLEARED.) THE "0" OUTPUT OF BØTSTATO FEEDS INF1400 AND THE ONE OUTPUT OF EØTSTAT1 FEEDS INF0800. THE TAPE POSITION STATUS WILL APPEAR AT THE OUTPUT OF THESE TWO GATES WHEN THEY ARE ENABLED BY A HIGH LEVEL OF SSTAT1. THE TAPE POSITION STATUS INFORMATION APPEARS ON THE INF140 AND INF080 LEADS AS FOLLOWS:

C. TAPE STATUS INFORMATION	INF140	INF08D
BEGINNING OF TAPE, NONWRITEABLE AREA	LOW	HIGH
WRITEABLE AREA	HIGH	HIGH
END OF TAPE, NONWRITNG AREA	HIGH	LOW

A 768KHZ CRYSTAL OSCILLATOR ØCS IS USED IN THE CTTC WRITE CLOCK. THE OUTPUT IS FED INTO A 4-BIT COUNTER DIVCLK. THE OUTPUT OF THE MOST SIGNIFICANT BIT OF THIS COUNTER, A 48KHZ SQUARE WAVE, IS FED INTO THE TOW MONOPULSERS CLK01 AND CLKD2. CLKD1 IS TRIGGERED ON EVERY HIGH-GOING EDGE OF THIS SQUARE WAVE AND CLK02 IS TRIGGERED ON EVERY GROUND GOING EDGE. THE OUTPUT OF BOTH THESE MONOPULSERS IS A STREAM OF 1μs HIGH-GOING PULSES OCCURING AT A FREQUENCY OF 48KHZ. THEY ARE 180° OUT OF PHASE WITH EACH OTHER SO THAT THE COMPOSITE OUTPUT IS A 48KHZ 2-PHASE CLOCK. OUTPUTS CLK011 AND CLK021 ARE FED TO THE WRITE CIRCUIT LOCATED ON JK18.

THE OUTPUT OF THE SECOND MOST SIGNIFICANT BIT OF DIVCLK ØSCBFR IS A 96KHZ SQUARE WAVE, WHICH IS USED TO CLOCK THE WRITE DELAY CIRCUIT. THE WRITE DELAY CIRCUIT IS BASICALLY THREE 41CJ 4-BIT COUNTERS, WDCTR1, WDCTR2, AND WDCTR3. THE ET AND THE EP INPUTS TO WDCTR1, THE ET INPUT TO WDCTR2, AND THE LOAD INPUTS TO ALL THREE COUNTERS ARE HELD AT A CONSTANT HIGH-LEVEL BY HILVL1. THE LOAD, ET AND EP INPUTS, MUST ALL BE HIGH BEFORE THE 41CJ WILL COUNT. THEREFORE WDCTR1 WILL COUNT ON EVERY CYCLE OF THE 96KHZ SQUARE WAVE. THE CARRY OUTPUT WDCTR1 FEEDS THE EP INPUT OF WDCTR2, OF THEREFORE, WDCTR2 WILL ONLY COUNT EVERY 16TH CYCLE OF THE SQUARE WAVE (THE CARRY OUTPUT OF WDCTR1 IS HIGH ONLY EVERY SIXTEENTH CYCLE). WDCTR3 WILL ONLY COUNT EVERY TWO-HUNDRED AND FIFTY-SIXTH CYCLE OF THE SQUARE WAVE SINCE ITS ET INPUT IS ENABLED BY THE CARRY OUTPUT OF WDCTR2 AND ITS EP INPUT IS ENABLED BY THE CARRY OUTPUT OF WDCTR1. THE CONFIGURATIONS DESCRIBED ABOVE MAKE UP A SINGLE 10-BIT COUNTER. THE COUNTER IS STARTED BY A PULSE APPEARING ON THE WRITEO LEAD. THIS PULSE IS GENERATED BY CIRCUITS ON JK16 IN RESPONSE TO THE CTTC RECEIVING A WRITE COMMAND. THIS PULSE SETS THE 12-BIT COUNTER TO ITS ZERO STATE (ALL CARRY OUTPUTS ARE LOW) WHICH INSURES A HIGH LEVEL AT THE OUTPUT OF WRITEP1. THIS HIGH LEVEL FORCES THE OUTPUT OF WRITEPO LOW AND ENABLES WDCNTBO. THE LOW SIGNAL AT THE OUTPUT OF WRITEPO IS FED TO THE WRITE CIRCUIT ON JK18. THE WRITE CIRCUIT WILL REMAIN IN ITS INTERRECORD GAP STATE AS LONG AS WRITEPO IS LOW (SEE THE CIRCUIT DESCRIPTION OF JK18 FOR FURTHER EXPLANATION). ENABLING WDCNTBO ALLOWS THE INVERTED 96KHZ SQUARE WAVE ON ØSCBFR TO APPEAR AT THE CLOCK INPUTS TO THE COUNTER. AFTER 4095 CYCLES OF THE SQUARE WAVE 42.59ms, ALL THREE CARRY OUTPUTS WILL BE AT A HIGH LEVEL. THESE THREE HIGH LEVELS FORCE THE OUTPUT OF WRITEP1 LOW. THE LOW OUTPUT FROM WRITEP1 DISABLES WDCNTBO, INHIBITING THE SQUARE WAVE INPUT TO THE COUNTER. THE HIGH LEVEL AT THE OUTPUT OF WRITEPO ALLOWS THE WRITE CIRCUIT TO START TRANSMITTING DATA TO THE CTT. THE CIRCUIT DESCRIBED ABOVE PROVIDES A 42.59ms LOW-GOING PULSE (WRITE-DELAY PULSE) AT THE OUTPUT OF WRITPO. THE NORMAL STATE OF THIS DELAY CIRCUIT IS A HIGH-CARRY OUTPUT FROM ALL THREE COUNTERS. IF THEY ARE NOT IN THIS STATE WHEN POWER IS APPLIED, WDCNTBO IS ENABLED, ALLOWING THE SQUARE WAVE INPUT TO CYCLE THEM TO THAT STATE. WDCNTBO WILL BE DISABLED WHEN A FULL COUNT IS REACHED.